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Figure 10A is a cross-sectional view of a semiconductor device 10A. The device features a substrate 11A with a central layer 12. A gate structure 13 is formed on the substrate, with a gate dielectric 14 and a gate electrode 15. A source/drain region 16 is formed in the substrate, with a source/drain dielectric 17A and a source/drain electrode 18. A contact pad 19 is formed on the source/drain electrode. A cross-section line X-X' is indicated.

FIG. 1 is a schematic diagram of a square-shaped semiconductor device. The device features a central square region (12) surrounded by a rectangular frame (11A). The frame is composed of four sides, each with a series of circular pads (13) and rectangular pads (16). A central pad (21) is located at the top-left corner of the frame. Arrows indicate electrical connections between the pads and the central region.

[illegible]

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FIG.3

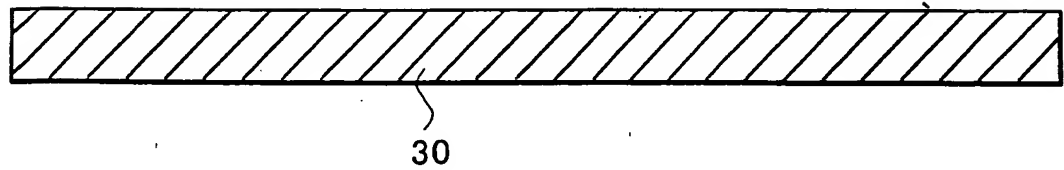


FIG.4

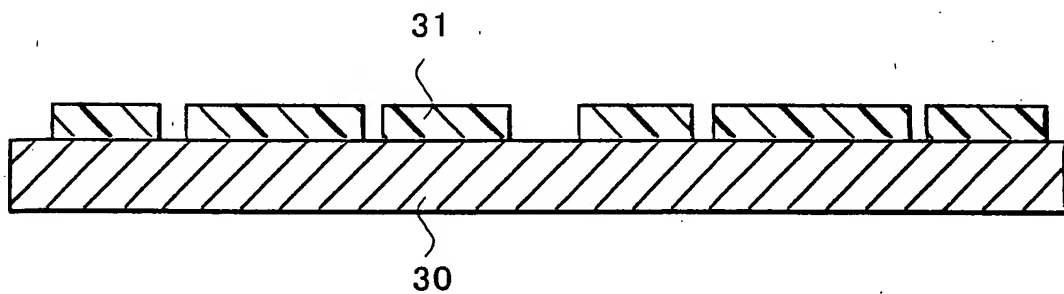


FIG.5

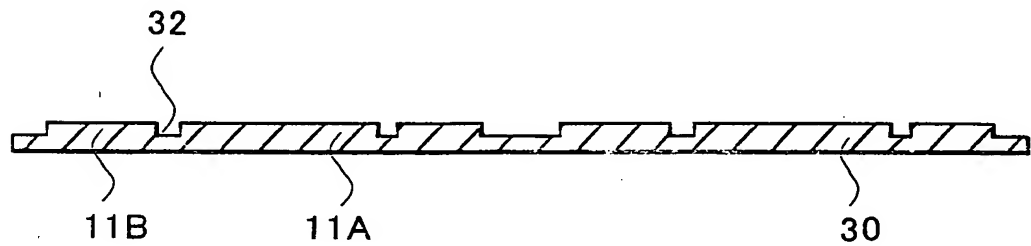
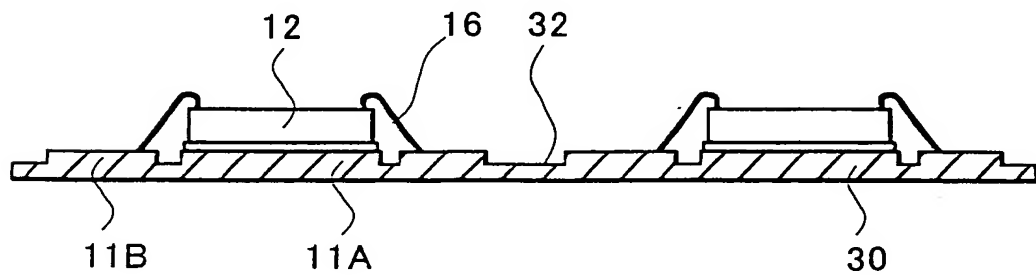


FIG.6



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FIG. 7

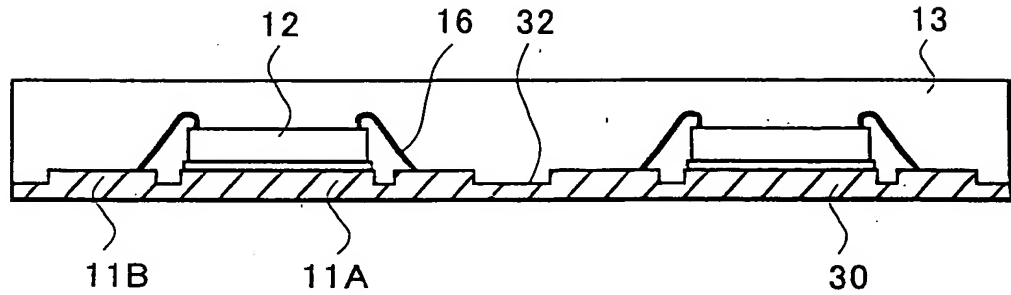


FIG. 8

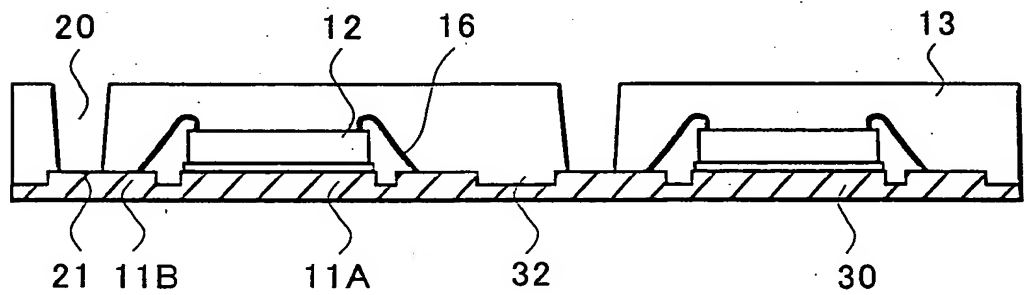
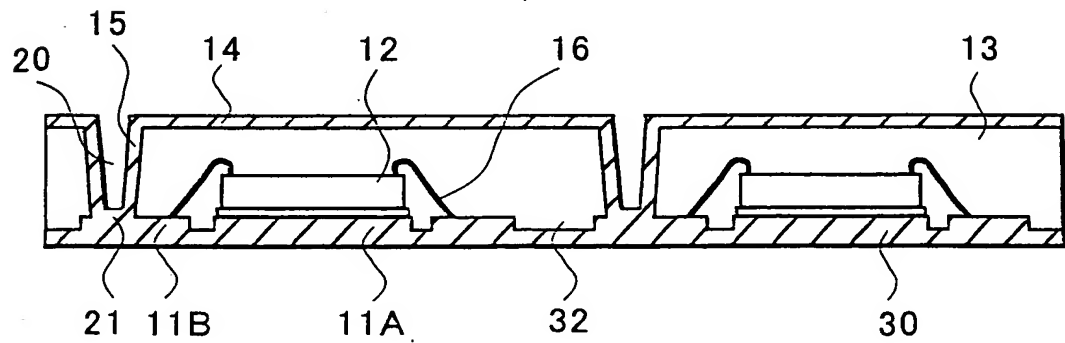


FIG. 9



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FIG.10

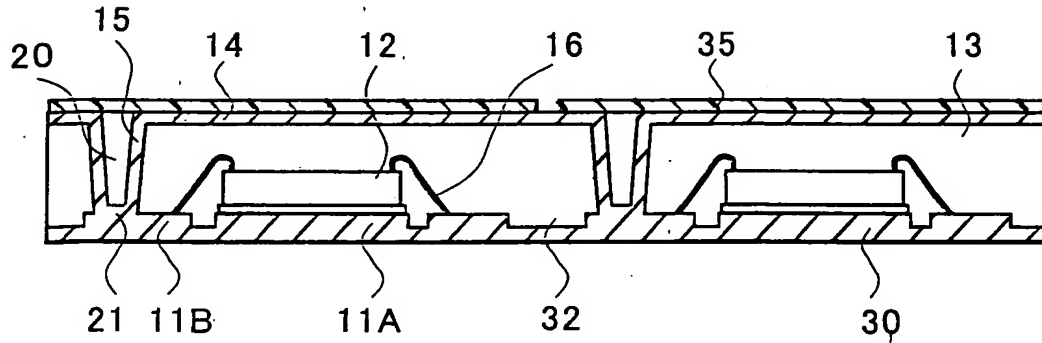


FIG.11

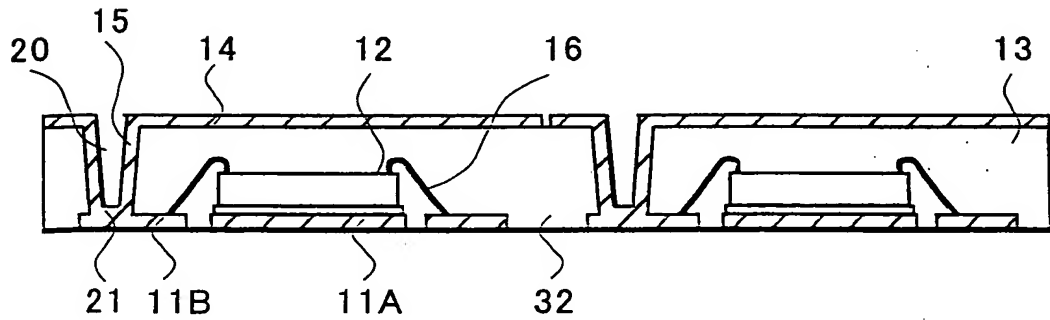
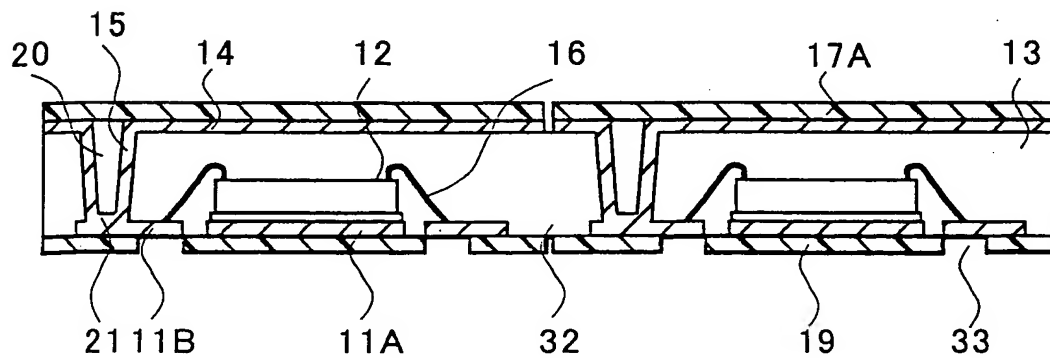


FIG.12



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FIG.13

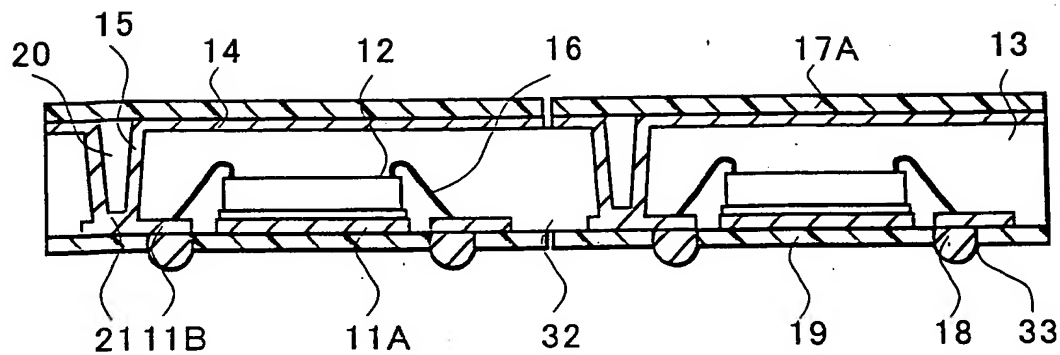
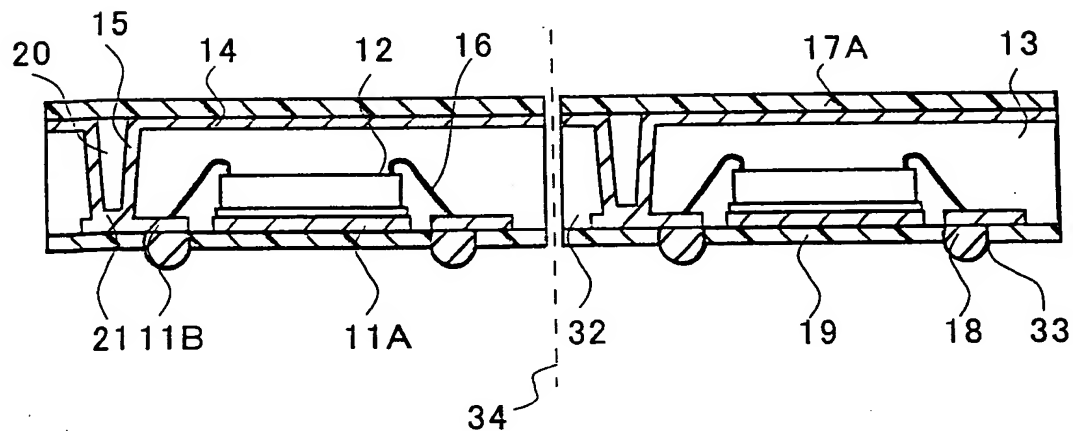


FIG.14



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FIG.15

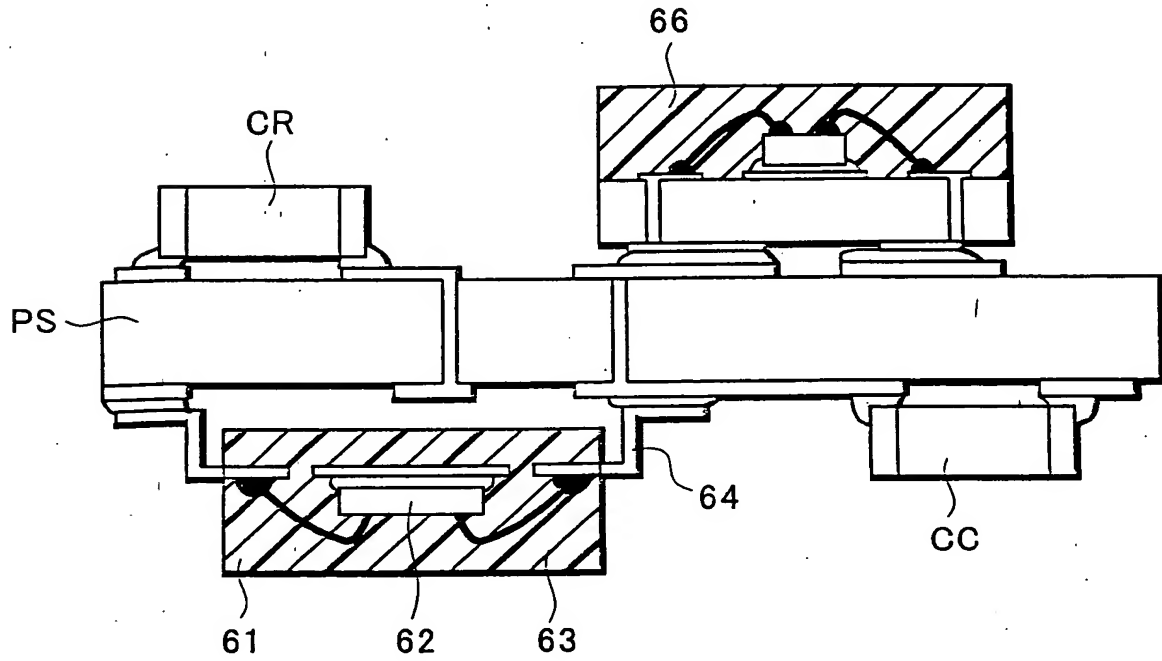


FIG.16

